Customer No.: 31561
Application No.: 10/065,919
Docket No.: 9817-US-PA

REMARKS

Present Status of the Application

The Office Action rejected presently pending claims 1-4, 6, 9, 10, 12, 15-18 and 20, and objected presently pending claims 5, 7, 8, 11, 13, 14 and 19. Specifically, the Office Action rejected claims 15-17 under 35 U.S.C. 102(e), as being anticipated by Shen et al. (U.S. 6,486,067 B1). The Office Action rejected claims 1-3, 6, 9 and 12 under 35 U.S.C. 103(a), as being unpatentable over Yang et al. (U.S. 6,515,328 B1) in view of So (U.S. 6,136,666). The Office Action rejected claims 18 under 35 U.S.C. 103(a), as being unpatentable over Yang et al. (U.S. 6,515,328 B1) in view of Lee (U.S. 6,124,153). The Office Action rejected claims 4 and 10 under 35 U.S.C. 103(a), as being unpatentable over Yang et al. (U.S. 6,515,328 B1) and So (U.S. 6,136,666) in view of Lee (U.S. 6,124,153). Applicants have amended claims 1, 9 and 15 without adding new matters. After entry of the foregoing amendments, claims 1-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 15-17 under 35 U.S.C. 102(e), as being anticipated by Shen et al. (U.S. 6,486,067 B1). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claim 15 and claim 16 recite the features as follows:

15. A re-oxidation process of a semiconductor device, comprising:
providing a substrate having a stacked structure thereon, wherein the stacked structure includes a polysilicon/metal silicide interface;
forming a CVD oxide layer on both the substrate and the stacked structure with a chemical vapor deposition (CVD) process; and
performing an oxidation process to form a thermal oxide layer on both the substrate and the stacked structure.

(emphasis added).

16. The re-oxidation process of claim 15, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a tunneling layer, a polysilicon floating gate, ***an inter-poly dielectric layer***, ***a polysilicon control gate*** and a metal silicide layer.

(emphasis added).

In Shen et al., especially in Col. 3, line 8-30 and FIG. 5A-5B, Shen et al. only disclose that "...the edges of the polysilicon layer 18 **are oxidized**, and **also** the edges of tungsten silicide layer 20. **This oxidation results in a thickened layer portion 21** of electrically conductive tungsten silicide that ....." . Therefore, Applicants assert that Shen et al. DO NOT disclosed **a CVD oxide layer formation process**.

sequentially forming a tunneling layer, a first polysilicon layer, an inter-poly dielectric layer, a second polysilicon layer and a tungsten silicide layer on a substrate;

sequentially patterning the tungsten silicide layer, the second polysilicon layer, the inter-poly dielectric layer and the first polysilicon layer to form a stacked gate;

forming a CVD oxide layer on ***both the substrate and the stacked gate*** with a chemical vapor deposition (CVD) process; and

performing an oxidation process to form a thermal oxide layer on the substrate and the stacked gate.

(emphasis added).

Claim 2, 3, 6 and 12 also recite the similar features

In Yang et al. (as shown in FIG. 7), Applicants assert that Yang et al. fail to disclose the feature of "forming a CVD oxide layer on ***both the substrate and the stacked gate*** with a chemical vapor deposition (CVD) process" as claimed in claim 1 and 9. Specifically, in FIG. 7, the silicon oxynitride layer 68 is formed only on the top surface of the cap layer 66, both the substrate 12 and sidewalls of the stacked structure (62, 64, 66, 68) are not covered by the silicon oxynitride layer 68. However, according to Applicants' specification (page 5, paragraph 20), the CVD oxide layer of present invention can prevent fast oxidation on exposed surfaces of the tungsten silicide layer and the polysilicon layer, (i.e. sidewalls of the stacked structure is covered by the CVD oxide layer, which is support in FIG. 1B of present invention). Hence, Applicants assert that there is no motivation to combine these prior arts because the "fast oxidation"

Also, Applicants consider that Shen et al. DO NOT disclose a stacked structure claimed in the Claim 16. Specifically, the stacked structure disclosed by Shen et al. merely comprises a gate oxide layer 16, a first polysilicon layer 18, a first metal silicide layer 20 and a first insulating layer 22, ***an inter-poly dielectric layer*** and ***a polysilicon control gate*** are not disclosed by Shen et al. Therefore, the prior art disclosed by Shen et al. is different from the Claims 15-17, and reconsideration of claims 15-17 is respectfully requested.

The Office Action rejected claims 1-3, 6, 9 and 12 under 35 U.S.C. 103(a), as being unpatentable over Yang et al. (U.S. 6,515,328 B1) in view of So et al. (U.S. 6,136,666). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claim 1 and 9 recite the features as follows:

> 1. A rc-oxidation process of a semiconductor device, comprising:
> providing a substrate having a stacked structure thereon, wherein the stacked structure includes a polysilicon/tungsten silicide interface
> ***forming a CVD oxide layer on both the substrate and the stacked structure with a chemical vapor deposition (CVD) process; and***
> performing an oxidation process to form a thermal oxide layer on both the substrate and the stacked structure.
>
> (emphasis added).
>
> 9. A method for fabricating a semiconductor device, comprising:

phenomenon would not occur in the structures shown in the prior arts. On the other hand, So et al. disclose a first oxide film 11 only, but the first oxide film 11 is formed on the first silicon substrate 10 by thermal oxidation process (Col.1, lines 46+). Therefore, it is difficult for a skilled artisan to form a thermal oxide layer on the stacked structure without proper suggestions or teachings.

Even the Examiner insists that the combination can be accomplished, the combination of these prior arts is still different from claims 1 and 9. Not all the elements defined in claim 1 and 9 are disclosed in the prior arts, such as "a CVD oxide layer on ***both the substrate and the stacked gate***" etc. Accordingly, claim 1 and 9 are non-obvious over Yang et al. (U.S. 6,515,328 B1) in view of So et al. (U.S. 6,136,666).

For at least the foregoing reasons, Applicants respectfully submit that independent claims 1 and 9 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2, 3, 6 and 12 patently define over the prior art as well.

The Office Action rejected claims 18 under 35 U.S.C. 103(a), as being unpatentable over Yang et al. (U.S. 6,515,328 B1) in view of Lee (U.S. 6,124,153). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Customer No.: 31561
Application No.: 10/065,919
Docket No.: 9817-US-PA

Applicants submit that Yang et al. fail to disclose all the features of the claimed invention as discussed above. Therefore, even the Examiner insists that the combination can be accomplished, the combination of these prior arts is still different from claim 18. Not all the elements defined in claim 18 are disclosed in the prior arts (Yang and Lee), such as "a CVD oxide layer on ***both the substrate and the stacked gate***" etc. Accordingly, claim 18 are non-obvious over Yang et al. (U.S. 6,515,328 B1) in view of Lee (U.S. 6,124,153).

The Office Action rejected claims 4 and 10 under 35 U.S.C. 103(a), as being unpatentable over Yang et al. (U.S. 6,515,328 B1) and So (U.S. 6,136,666) in view of Lee (U.S. 6,124,153). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Applicants submit that Yang et al. and So et al. fail to disclose all the features of the claimed invention as discussed above. Therefore, even the Examiner insists that the combination can be accomplished, the combination of these prior arts (Yang, So and Lee) is still different from claims 4 and 10. Not all the elements defined in claim 4 and 10 are disclosed in the prior arts. Accordingly, claim 4 and 10 are non-obvious over Yang et al. (U.S. 6,515,328 B1) and So et al. in view of Lee (U.S. 6,124,153).

For at least the foregoing reasons, Applicant respectfully submits that dependent claim 4 and 10 patently define over the prior art references, and should be allowed.

The Office Action rejected claim 20 under 35 U.S.C. 103(a), as being unpatentable over Yang et al. (U.S. 6,515,328 B1) in view of So (U.S. 6,136,666). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Applicants submit that Yang et al. and So et al. fail to disclose all the features of the claimed invention as discussed above. Furthermore, So discloses "A first oxide film 31 with thickness of ***500 ~ 1000Å*** is formed on one side of the first silicon substrate 30 ***by a thermal oxidation process***". In other words, the first oxide film 31 disclosed by So is a ***thermal oxide layer***, not a ***CVD oxide layer***. Therefore, Applicants assert that So fail to disclose, teach or suggest "the ***CVD oxide layer*** has a thickness of ***30 ~ 120Å***" as claimed in claim 20. Accordingly, claim 20 are non-obvious over Yang et al. in view of So.

For at least the foregoing reasons, Applicants respectfully submit that dependent claim 20 patently define over the prior art references, and should be allowed.

Customer No.: 31561
Application No.: 10/065,919
Docket No.: 9817-US-PA

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw